	Typ	Hits	Search T xt	DBs	Time Stamp
1	BRS	2	6717216.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/20 17:08
2	BRS	0	6717216.URPN.	USPAT	2004/05/20 17:09
3	BRS	2	("6376286" | "6472258").PN.	USPAT	2004/05/20 17:09
4	BRS	2	6573561.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/20 17:11
5	BRS	774	implant$5 with (He Ar noble) same substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:51
6	BRS	114	(implant$5 with (He Ar noble) same substrate) and (implant$5 with (oxygen or (O?sub?2)) same substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/20 17:29
7	BRS	4364	(implant$5 with (oxygen or (O?sub?2)) same substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/20 17:13
8	BRS	75	(implant$5 with (He Ar noble) same substrate) and (implant$5 with (oxygen or (O?sub?2)) same substrate) and anneal$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:30
9	BRS	1192	expand$3 with substrate and compress$3 with substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/20 17:28
10	BRS	1	(implant$5 with (He Ar noble) same substrate) and (implant$5 with (oxygen or (O?sub?2)) same substrate) and (expand$3 with substrate and compress$3 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:08
11	BRS	0	(implant$5 with (He Ar noble) same substrate) and (expand$3 with substrate same compress$3 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:34
12	BRS	564	expand$3 with substrate same compress$3 with substrate	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:32
13	BRS	30	(implant$5 with substrate) and (expand$3 with substrate same compress$3 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:21
14	BRS	2328	NFET and PFET	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:01
15	BRS	27048	PMOS and NMOS	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:21
16	BRS	249	(NFET and PFET) and (PMOS and NMOS)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:21

	Type	Hits	Search T xt	DBs	Tim Stamp
17	BRS	31	(implant$5 with substrate) and ((NFET and PFET) and (PMOS and NMOS))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:21
18	BRS	151	(implant$5 with (He Ar noble) with substrate) and (implant$5 with (oxygen or (O?sub?2)) withsame substrate) and anneal$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:31
19	BRS	42	(implant$5 with (He Ar noble) with substrate) and (implant$5 with (oxygen or (O?sub?2)) with substrate) and anneal$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:31
20	BRS	11880	((compress$3 or shrink$3 or reduc$4 or condens$3) with substrate) and (implant$5 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:34
21	BRS	54	(implant$5 with (He Ar noble) same substrate) and (((compress$3 or shrink$3 or reduc$4 or condens$3) adj5 substrate) and (implant$5 with substrate))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:49
22	BRS	2	6261876.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:49
23	BRS	2	6541356.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:49
24	BRS	119	implant$5 with (He Ar noble) same substrate same anneal$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 16:52
25	BRS	59	implant$5 with (He Ar noble) with substrate same anneal$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:01
26	BRS	197	438/153.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:00
27	BRS	198	438/216.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:00
28	BRS	142	438/225.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:00
29	BRS	1080	438/439.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:00
30	BRS	88	438/440.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:00
31	BRS	2	NFET and PFET and PMOS and NMOS and 438/153.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:01

	Typ	Hits	Search Text	DBs	Time Stamp
32	BRS	11	implant$5 with substrate same anneal$3 and 438/153.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/23 17:02
33	BRS	7	6436771.URPN.	USPAT	2004/05/23 17:03
34	BRS	2	6306721.URPN.	USPAT	2004/05/23 17:04
35	BRS	14	4987092.URPN.	USPAT	2004/05/23 17:04
36	BRS	45591	((compress$3 or shrink$3 or reduc$4 or condens$3) adj5 substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:37
37	BRS	3333	((compress$3 or shrink$3 or reduc$4 or condens$3) adj5 substrate) and (implant$5 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:37
38	BRS	750	((compress$3 or shrink$3 or reduc$4 or condens$3) adj5 substrate) same (implant$5 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:36
39	BRS	330	((compress$3 or shrink$3 or condens$3) adj5 substrate) and (implant$5 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:37
40	BRS	9873	((compress$3 or shrink$3 or condens$3) adj5 substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:37
41	BRS	28	((compress$3 or shrink$3 or condens$3) adj5 substrate) same (implant$5 with substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:37
42	BRS	2	("5075242" | "5955767").PN.	USPAT	2004/05/27 16:38
43	BRS	3	6228694.URPN.	USPAT	2004/05/27 16:39
44	BRS	0	chidambarrao.iv	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:49
45	BRS	50	chidambarrao.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 16:49
46	BRS	2	("6376286" | "6472258").PN.	USPAT	2004/06/12 19:22
47	BRS	2	6261876.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/12 19:52
48	BRS	1	6261876.URPN.	USPAT	2004/06/12 19:52

	Type	Hits	S arch Text	DBs	Tim Stamp
49	BRS	16	("5343064" | "5344787" | "5494846" | "5631186" | "5811283" | "5877048" | "5877978" | "5892256" | "5894152" | "5904535" | "6096582" | "6096583" | "6107125" | "6127242" | "6174784" | "6194253").PN.	USPAT	2004/06/12 19:53
50	BRS	2	6541356.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/12 19:54
51	BRS	0	6541356.URPN.	USPAT	2004/06/12 19:54
52	BRS	15	("4749660" | "4786608" | "4902642" | "4975126" | "5182226" | "5279978" | "5288650" | "5519336" | "5589407" | "5712186" | "5895252" | "5930643" | "6043166" | "6090689" | "6214653").PN.	USPAT	2004/06/12 19:54

PALM INTRANET

Day : Thursday
Date: 5/20/2004
Time: 17:04:23

Inventor Name Search Result

Your Search was:

Last Name = CHIDAMBARRAO
First Name = DURESETI

Application#	Patent#	Status	Date Filed	Title	Inventor Name 51
10790550	Not Issued	020	03/01/2004	METHOD OF MANUFACTURE OF FINFET DEVICES WITH T-SHAPED FINS AND DEVICES MANUFACTURED THEREBY	CHIDAMBARRAO, DURESETI
10751916	Not Issued	019	01/07/2004	HIGH PERFORMANCE STRAINED SILICON FINFETS DEVICE AND METHOD FOR FORMING SAME	CHIDAMBARRAO, DURESETI
10733381	Not Issued	030	12/12/2003	STRUCTURE AND METHOD FOR ULTRA-SMALL GRAIN SIZE POLYSILICON	CHIDAMBARRAO, DURESETI
10733378	Not Issued	020	12/12/2003	STRAINED FINFETS AND METHOD OF MANUFACTURE	CHIDAMBARRAO, DURESETI
10730234	Not Issued	020	12/09/2003	PULL-BACK METHOD OF FORMING FINS IN FINFETS	CHIDAMBARRAO, DURESETI
10728750	Not Issued	030	12/08/2003	DYNAMIC THRESHOLD VOLTAGE MOSFET ON SOI	CHIDAMBARRAO, DURESETI
10715400	Not Issued	030	11/19/2003	SILICON DEVICE ON SI:C-OI AND SGOI AND METHOD OF MANUFACTURE	CHIDAMBARRAO, DURESETI
10709450	Not Issued	019	01/01/0001	OUT OF THE BOX VERTICAL TRANSISTOR FOR EDRAM ON SOI	CHIDAMBARRAO, DURESETI
10708746	Not Issued	020	03/23/2004	STRAINED SILICON NMOS DEVICES WITH EMBEDDED	CHIDAMBARRAO, DURESETI

				SOURCE/DRAIN	
10708381	Not Issued	020	02/27/2004	GATE CONTROLLED FLOATING WELL VERTICAL MOSFET	CHIDAMBARRAO, DURESETI
10707018	Not Issued	030	11/14/2003	STRESSED SEMICONDUCTOR DEVICE STRUCTURES HAVING GRANULAR SEMICONDUCTOR MATERIAL	CHIDAMBARRAO, DURESETI
10706061	Not Issued	030	11/13/2003	STRAINED SILICON ON A SIGE ON SOI SUBSTRATE	CHIDAMBARRAO, DURESETI
10695752	Not Issued	030	10/30/2003	STRUCTURE AND METHOD TO IMPROVE CHANNEL MOBILITY BY GATE ELECTRODE STRESS MODIFICATION	CHIDAMBARRAO, DURESETI
10689506	Not Issued	030	10/20/2003	HIGH PERFORMANCE STRESS-ENHANCED MOSFETS USING SI:C AND SIGE EPITAXIAL SOURCE/DRAIN AND METHOD OF MANUFACTURE	CHIDAMBARRAO, DURESETI
10687608	Not Issued	030	10/20/2003	STRAINED DISLOCATION-FREE CHANNELS FOR CMOS AND METHOD OF MANUFACTURE	CHIDAMBARRAO, DURESETI
10682430	Not Issued	030	10/10/2003	HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER	CHIDAMBARRAO, DURESETI
10669727	Not Issued	041	09/25/2003	FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME	CHIDAMBARRAO, DURESETI
10667603	Not Issued	020	09/23/2003	STRAINED SILICON ON RELAXED SIGE FILM WITH UNIFORM MISFIT DISLOCATION DENSITY	CHIDAMBARRAO, DURESETI
10667601	Not Issued	071	09/23/2003	NFETS USING GATE INDUCED STRESS MODULATION	CHIDAMBARRAO, DURESETI

10605310	Not Issued	030	09/22/2003	SILICIDE PROXIMITY STRUCTURES FOR CMOS DEVICE PERFORMANCE IMPROVEMENTS	CHIDAMBARRAO, DURESETI
10605227	Not Issued	071	09/16/2003	METHOD AND STRUCTURE OF VERTICAL STRAINED SILICON DEVICES	CHIDAMBARRAO, DURESETI
10605167	Not Issued	071	09/12/2003	MOSFET PERFORMANCE IMPROVEMENT USING DEFORMATION IN SOI STRUCTURE	CHIDAMBARRAO, DURESETI
10605135	Not Issued	030	09/10/2003	METHOD AND STRUCTURE FOR IMPROVED MOSFETS USING POLY/SILICIDE GATE HEIGHT CONTROL	CHIDAMBARRAO, DURESETI
10605134	Not Issued	020	09/10/2003	STRUCTURE AND METHOD OF MAKING STRAINED CHANNEL CMOS TRANSISTORS HAVING LATTICE-MISMATCHED EPITAXIAL EXTENSION AND SOURCE AND DRAIN REGIONS	CHIDAMBARRAO, DURESETI
10605108	Not Issued	041	09/09/2003	METHOD FOR REDUCED N+ DIFFUSION IN STRAINED SI ON SIGE SUBSTRATE	CHIDAMBARRAO, DURESETI
10604731	Not Issued	030	08/13/2003	SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING	CHIDAMBARRAO, DURESETI
10604607	Not Issued	030	08/04/2003	STRUCTURE AND METHOD OF MAKING STRAINED SEMICONDUCTOR CMOS TRANSISTORS HAVING LATTICE-MISMATCHED SOURCE AND DRAIN REGIONS	CHIDAMBARRAO, DURESETI
10604190	Not Issued	030	06/30/2003	HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF	CHIDAMBARRAO, DURESETI

				MANUFACTURE	
10441887	Not Issued	041	05/20/2003	TRENCH CAPACITORS WITH REDUCED POLYSILICON STRESS	CHIDAMBARRAO, DURESETI
10341831	6734056	150	01/14/2003	SELF-ALIGNED PUNCH THROUGH STOP FOR 6F2 ROTATED HYBRID DRAM CELL	CHIDAMBARRAO, DURESETI
10340999	6724031	150	01/13/2003	METHOD FOR PREVENTING STRAP-TO-STRAP PUNCH THROUGH IN VERTICAL DRAMS	CHIDAMBARRAO, DURESETI
10336988	6703274	150	01/03/2003	BURIED STRAP WITH LIMITED OUTDIFFUSION AND VERTICAL TRANSISTOR DRAM	CHIDAMBARRAO, DURESETI
10318602	Not Issued	061	12/12/2002	STRESS INDUCING SPACERS	CHIDAMBARRAO, DURESETI
10318601	6717216	150	12/12/2002	FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME	CHIDAMBARRAO, DURESETI
10318600	Not Issued	020	12/12/2002	ISOLATION STRUCTURES FOR IMPOSING STRESS PATTERNS	CHIDAMBARRAO, DURESETI
10290400	6707095	150	11/06/2002	STRUCTURE AND METHOD FOR IMPROVED VERTICAL MOSFET DRAM CELL-TO-CELL ISOLATION	CHIDAMBARRAO, DURESETI
10265558	Not Issued	030	10/04/2002	STRUCTURE AND METHOD OF VERTICAL TRANSISTOR DRAM CELL HAVING A LOW LEAKAGE BURIED STRAP	CHIDAMBARRAO, DURESETI
10250259	Not Issued	093	06/18/2003	TRENCH CAPACITOR DRAM CELL USING BURIED OXIDE AS ARRAY TOP OXIDE	CHIDAMBARRAO, DURESETI
10248819	Not Issued	071	02/21/2003	CMOS PERFORMANCE ENHANCEMENT USING LOCALIZED VOIDS AND EXTENDED DEFECTS	CHIDAMBARRAO, DURESETI
10243540	Not Issued	061	09/13/2002	STRUCTURE AND METHOD OF PROVIDING	CHIDAMBARRAO, DURESETI

				REDUCED PROGRAMMING VOLTAGE ANTIFUSE	
10160540	6709926	150	05/31/2002	HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER	CHIDAMBARRAO, DURESETI
10096219	6740920	150	03/11/2002	VERTICAL MOSFET WITH HORIZONTALLY GRADED CHANNEL DOPING	CHIDAMBARRAO, DURESETI
10096192	6573561	150	03/11/2002	VERTICAL MOSFET WITH ASYMMETRICALLY GRADED CHANNEL DOPING	CHIDAMBARRAO, DURESETI
10078926	6534824	150	02/20/2002	SELF-ALIGNED PUNCH THROUGH STOP FOR 6F2 ROTATED HYBRID DRAM CELL	CHIDAMBARRAO, DURESETI
10016605	Not Issued	093	10/30/2001	VERTICAL DRAM PUNCHTHROUGH STOP SELF-ALIGNED TO STORAGE TRENCH	CHIDAMBARRAO, DURESETI
09904612	6653678	150	07/13/2001	REDUCTION OF POLYSILICON STRESS IN TRENCH CAPACITORS	CHIDAMBARRAO, DURESETI
09769494	6548358	150	01/26/2001	ELECTRICALLY BLOWABLE FUSE WITH REDUCED CROSS-SECTIONAL AREA	CHIDAMBARRAO, DURESETI
09769453	6573585	150	01/26/2001	ELECTRICALLY BLOWABLE FUSE WITH REDUCED CROSS-SECTIONAL AREA	CHIDAMBARRAO, DURESETI
08667210	5729052	150	06/20/1996	INTEGRATED ULSI HEATSINK	CHIDAMBARRAO , DURESETI
08166415	5470781	150	12/14/1993	METHOD TO REDUCE STRESS FROM TRENCH STRUCTURE ON SOI WAFER	CHIDAMBARRAO , DURESETI
07809357	Not Issued	161	12/17/1991	ALPHA PARTICLE DISTURB REDUCTION TECHNIQUES	CHIDAMBARRAO , DURESETI

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